Customer No.: 31561
Docket No.: 10070-US-PA
Application No.: 10/707,012

REMARKS

Present Status of the Application

The Office Action rejected claims 1, 7, 13 and 15-16 under 35 U.S.C. 103(a) as being unpatentable over Sato (US 2002/0140643) in view of Kunori (US 6,144,584). The Office Action rejected claims 2, 8 and 14 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Lee (US 6,133,103). The Office Action rejected claims 3 and 9 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Lai (US 6,875,645). The Office Action rejected claims 4, 10 and 17 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Tomisawa (US 4,742,254). The Office Action rejected claims 5 and 11 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori in view of Tomisawa and further in view of Lee. In addition, claims 6 and 12 are objected to as being dependent upon a rejected base claim.

Applicant has amended claims 1, 7 and 13 and cancelled claims 4, 10 and 17 to more clearly define the present invention. After entry of the foregoing amendments, claims 1-3, 5-9, 11-16 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Rejection under 35 U.S.C 103 (a)

The Office Action rejected claims 1, 7, 13 and 15-16 under 35 U.S.C. 103(a) as being unpatentable over Sato (US 2002/0140643) in view of Kunori (US 6,144,584). The Office

PAGE 6/13 * RCVD AT 9/1/2006 3:17:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-08

Action rejected claims 4, 10 and 17 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Tomisawa (US 4,742,254).

Currently, Applicant has added the limitation of claim 4 into claim 1; added the limitation of claim 10 into claim 7; and added the limitation of claim 17 into claim 13. Applicant respectfully traverses the rejections for at least the reasons set forth below.

> To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a structure of reducing source line resistance and a method of reducing source line resistance as claims 1, 7 and 13 recite:

Claim 1. A structure of reducing source line resistance, suitable for use in a light emitting diode display that comprises a plurality of pixels, each of which comprises a light emitting diode, a source and a source line for providing required power to drive the light emitting diode, the structure comprising:

an insulation layer on the source line, the insulation layer having at least two openings exposing two ends of a part of the source line; and

at least a conductive layer covering the insulation layer and electrically connected to the source line via the openings, such that the conductive layer and at least the part of the source line are connected in parallel;

wherein the source line further comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel.

Claim 7. A structure of reducing source line resistance, suitable for use in a light emitting diode display that comprises a plurality of pixels, each of which comprises a light emitting diode,

a source and a source line for providing required power to drive the light emitting diode, the structure comprising:

an insulation layer on the source line, the insulation layer having a plurality of openings exposing the source line; and

a conductive layer covering the insulation layer and electrically connected to the source line via the openings, such that the conductive layer and at least the part of the source line are connected in parallel,

wherein the source line further comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel.

Claim 13. A method of reducing source line resistance, suitable for use in a light emitting diode display that comprises a plurality of pixels, each of which comprises a light emitting diode, a source and a source line for providing required power to drive the light emitting diode, ***wherein the source line further comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel***, the method comprising:

forming an insulation layer on the source line;

forming a plurality of openings exposing the source line; and

forming a conductive layer covering the insulation layer and electrically connected to the source line via the openings, such that the conductive layer and at least the part of the source line are connected in parallel.

The office action stated Sato taken with Kunori does not teach the structure wherein the source line further comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel (originally recited in the claims 4, 10 and 17). Tomisawa teaches this feature at col. 4, lines 24-32. However, applicant respectfully disagrees. As a matter of fact, Tomisawa just teaches "a power source line 28 comprises branch lines 28b in a comb form which are lead out from a bus 28a to supply power source voltage VSS to each row 22 via terminals 28c. A power source line 30 comprises branch lines 30b in a comb form which are led out from a bus 30a to oppose the branch lines 28b in a staggered fashion and supplies each row 22 with power source voltage

VDD via terminals 30c. The delay time is controlled by such power source voltages VDD and VSS" at col. 4, lines 24-33. Tomisawa fails to teach or suggest ***the branch lines are for supplying the power to the light emitting diode of each pixel.*** That is, the branch lines are electrically connected to the light emitting diode of each pixel for supplying the power. Therefore, applicant respectfully submits Tomisawa, Sato and Kunori fail to teach each and every element in claims 1, 7 and 13.

For at least the foregoing reasons, Applicant respectfully submits a prima facie case of obviousness for claims 1, 7 and 13 has not been established by the Office Action. Independent claims 1, 7 and 13 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 15-16 patently define over the prior art as a matter of law.

The Office Action rejected claims 5 and 11 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori in view of Tomisawa and further in view of Lee(US 6,133,103). Applicant respectfully traverses the rejections for at least the reasons set forth below.

The office action stated the limitation of the conductive layer comprises at least a conductor formed over the major source lines recited in claims 5 and 11 has been disclosed at col. 4, lines 44-67, col. 5, lines 1-8 and Fig. 7A of the Lee reference (US 6,133,103). However, applicant respectfully disagrees. Lee teaches a method for fabricating a mask ROM that improves the level of uniformity of cell voltages by using a second anti-reflective layer having a

PAGE 9/13 * RCVD AT 9/1/2006 3:17:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-08

thickness exists on word lines such that threshold voltage of the cell transistor programmed by **an impurity ion implantation process are uniform** irrespective of the cell transistor position on the substrate (see col. 4, lines 4-11). Lee also described (at col. 6, lines 4-24) that an impurity is selectively implanted into the surface of the semiconductor substrate under the word lines of the opened portion, e.g., the channel region of the cell transistor intended to be programmed. Selectively implanting the impurity forms impurity layers 37a and 37b in the first and second regions a and b, respectively. At this time, the impurity is preferably of the same conductivity type as the semiconductor substrate 21, e.g., P-type. The impurity layers 37a and 37b have uniform concentration and depth even if they are spaced apart from each other in one semiconductor substrate. This is because only the second anti-reflective layer 33 having a uniform thickness exists on the respective word lines before forming the photoresist pattern 35. In other words, ***since only a single material layer having a uniform thickness exists over the channel regions of all cell transistors during the ion implantation process for programming, a projection range Rp of the ion implantation process is shown at a constant depth from the surface of the channel region.***

Therefore, Applicant respectfully submits the method disclosed by Lee is using anti-reflective layer having a thickness existing on word lines such that threshold voltage of the cell transistor programmed by an impurity ion implantation process are uniform, and thus the level of uniformity of cell voltages can be improved. Lee fails to teach the device comprises at least a conductor formed over the major source lines that ***reduces the resistance of source line***

so as to improve the voltage distribution uniformity of the pixel. Henco, Applicant respectfully submits that the citations do not teach claims 5 and 11.

In addition, in holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention (*Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001)). The objective and the manner of the Lee reference is much different from the other references, there is no suggestion, motivation, or teaching in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention.

The Office Action rejected claims 2, 8 and 14 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Lee (US 6,133,103). The Office Action rejected claims 3 and 9 under 35 U.S.C. 103(a) as being unpatentable over Sato and Kunori and further in view of Lai (US 6,875,645). Applicant respectfully traverses the rejections for at least the reasons set forth below.

Applicant submits that, as disclosed above, Sato, Kunori, Tomisawa and Lee fail to teach or suggest each and every element of claims 1, 7 and 13 from which claims 2-3, 8-9 and 14 depend. Lai cannot cure the deficiencies of Sato, Kunori, Tomisawa and Lee. Therefore, independent claims 1, 7 and 13 are patentable over Sato, Kunori, Tomisawa, Lee and Lai. For

PAGE 11/13 * RCVD AT 9/1/2006 3:17:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-08

at the least the same reasons, their dependent claims 2-3, 8-9 and 14 are also patentable as a matter of law.

PAGE 12/13 * RCVD AT 9/1/2006 3:17:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-08

Customer No.: 31561
Docket No.: 10070-US-PA
Application No.: 10/707,012

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Sept. 1, 2006

Belinda Lee

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: Usa@jcipgroup.com.tw
belinda@jcipgroup.com.tw

PAGE 13/13 * RCVD AT 9/1/2006 3:17:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-08